

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissionerfor Patents, P.O. Box 1450, Alexandria,



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

VA 22313-1450.

Patent Application

Applicant(s): K.L. Davison et al.

Docket No.:

4-7-23

Serial No.:

10/722,652

Filing Date:

November 26, 2003

Group:

2831

Examiner:

Hung V. Ngo

Title:

Methods and Apparatus for Integrated

Circuit Device Power Distribution via

Internal Wire Bonds

REPLY BRIEF

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313

Sir:

This Reply Brief is submitted in response to the Examiner's Answer dated March 13, 2006 in the above-referenced application.

STATUS OF CLAIMS

The Examiner in his Answer to the Appeal Brief filed by Applicants (hereinafter "Appellants") on October 18, 2005, asserts that the status of claims contained in the brief is incorrect. Appellants note that the Examiner has changed the status of claims from the final Office Action so that only claims 1-8, 14, 15 and 17-20 are rejected under 35 U.S.C. §102(e). The scope of the appeal has also been changed by the Examiner to include only the above-referenced claims.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The Examiner in his Answer to the Appeal Brief filed by Appellants on October 18, 2005, asserts that the statement on the grounds of rejection to be reviewed on appeal is substantially correct. Appellants note that the Examiner has changed the §102(e) rejection from the final Office Action to include only claims 1-8, 14, 15 and 17-20.

ARGUMENT

The Examiner in his Answer to the Appeal Brief filed by Appellants on October 18, 2005, reasserts his arguments that claims 1-8, 14, 15 and 17-20 are anticipated under 35 U.S.C. §102(e). Appellants respectfully disagree with the assertions presented by the Examiner in the Answer, for at least the reasons identified below, as well as for those reasons previously set forth in the Appeal Brief.

With regard to the issue of whether claims 1-8, 14, 15 and 17-20 are properly rejected under 35 U.S.C. §102(e) as being anticipated by Taylor, the Examiner's Answer contends that Taylor discloses all of the claim limitations recited in the subject claims. Appellants respectfully reassert that Taylor fails to disclose all the claim limitations of the subject claims for at least the reasons previously presented in the Appellants' Appeal Brief.

Appellants again assert that Taylor fails to disclose <u>at least one bond wire connecting at least</u> one of a plurality of bond pads, disposed in a peripheral region of the die, <u>with at least one internal</u> bus, disposed in an interior region of the die, as recited in independent claim 1.

On page 6 of the Examiner's Answer, the Examiner contends that "Taylor et al disclose at least one bond wire connecting at least one of a plurality of bond pads (304, 350 Fig 3b) (see Exhibit

A)..." As is commonly known in the art of the present invention, a bond wire typically refers to a thin wire used in a wire bonding process to interconnect semiconductor pads on a die to package leads. As is evident from Exhibit A of the Examiner's Answer, the Examiner fails to fully comprehend the concept of bond wires commonly known in the art. More specifically, Exhibit A fails to show any such bond wires, and thus, also fails to show a bond wire connecting a bond pad with an internal bus. Instead, the Examiner incorrectly labels as bond wires, elements of FIG. 3B that are clearly shown and described as metal traces. As previously described throughout the application, the responses and the Appeal Brief, the present invention is directed to a bond wire connection, instead of a metal trace connection for the purpose of lowering resistivity and reducing power distribution voltage drop that normally occurs in metal traces routed from bond pads to internal buses.

J

In the Examiner's Answer, the Examiner further cites column 3, lines 18-20 of Taylor where it states that "[e]ach C4 power bus 360 is electronically coupled to one or more wire bond pad power connections 350." However, this citation fails to provide any evidence of the existence of bond wires. Instead, this portion of Taylor only indicates that the power bus and bond pads are electronically coupled. While element 350 is defined as a "wire bond pad power connection," this label provides no evidence that a bond wire extends from the wire bond power connection internally to the power bus. Instead, as is common in the art, and as shown in FIG. 3C, such wire bond pads 304 enable bond wire connections from the wire bond pads to an external package lead frame. Therefore, Taylor fails to show or describe any internal bond wire connection with respect to internal nodes or an internal voltage bus.

Further, portions of Taylor are directly contrary to the contentions of the Examiner. In column 2, lines 64-65, Taylor specifically states that "[t]he wire bond pads 304 are coupled to the C4 pads 306 through the metal layers 330 and conductive vias 332." Additionally, in column 3, lines 48-50, Taylor states that "the wire bond power connections 350 are coupled to the C4 power buses 360 along a metal trace connecting two of the C4 power connections 340." Therefore, the disclosure of a trace connection instead of a bond wire connection directly teaches away from the invention recited in claim 1 of the present invention. Thus, Taylor fails to disclose a bond wire connecting a bond pad with an internal bus.

Independent claim 19 recites a plurality of bond pads and at least one internal bus connectable by at least one bond wire, and independent claim 20 recites the step of wire bonding the at least one peripheral bond pad to the at least one internal bus. Therefore, independent claims 19 and 20 are patentable for at least the reasons presented above with regard to independent claim 1. Dependent claims 2-8, 14, 15, 17 and 18 are patentable at least by virtue of their respective dependency from independent claim 1. Dependent claims 2-8, 14, 15, 17 and 18 also recite patentable subject matter in their own right.

For at least the reasons given above and those previously provided in Appellants' Appeal Brief, Appellants respectfully request withdrawal of the §102(e) rejection of claims 1-8, 14, 15 and 17-20. Appellants believe that claims 1-8, 14, 15 and 17-20 are patentable over Taylor. As such, the application is asserted to be in condition for allowance, and favorable action is respectfully solicited.

Respectfully submitted,

Date: May 8, 2006

Robert W. Griffith Attorney for Applicant(s)

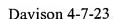
Reg. No. 48,956

Ryan, Mason & Lewis, LLP

90 Forest Avenue

Locust Valley, NY 11560

(516) 759-4547





IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. Box 1450,

atent Application

Applicant(s): K.L. Davison et al.

Case:

4-7-23

Serial No.:

10/722,652

Filing Date:

November 26, 2003

Group:

2831

Examiner:

Hung V. Ngo

Title:

Methods and Apparatus for Integrated

Circuit Device Power Distribution via

Internal Wire Bonds

TRANSMITTAL OF REPLY BRIEF

Mail Stop Appeal Brief - Patents Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

Submitted herewith is the following document relating to the above-identified patent application:

(1) Reply Brief.

It is believed that there is no additional fee due in conjunction with the response. In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit Ryan, Mason & Lewis, LLP Account No. 50-0762 as required to correct the error.

Respectfully submitted,

Date: May 8, 2006

Robert W. Griffith

Attorney for Applicant(s)

Reg. No. 48,956

Ryan, Mason & Lewis, LLP

90 Forest Avenue

Locust Valley, NY 11560

(516) 759-4547